ABSTRACT OF THE DISCLOSURE

A multi-level current pulse generator for driving the gates of a CMOS pair implemented using a low voltage process including a multi-level pulse translator, a current amplifier circuit, and a clamp circuit. The multi-level pulse translator generates a multi-level current pulse on at least one pulse node, each current pulse having a first large current pulse with short duration followed by at least one smaller current pulse of longer duration and operative to switch the CMOS pair with reduced average power dissipation. The current amplifier circuit amplifies the current pulses provided to the gates of the CMOS pair. The clamp circuit clamps gate voltage of the CMOS pair to prevent breakdown. In a tri-level case, a first current pulse charges and discharges gate capacitance, a second current pulse stabilizes gate voltage, and a third current pulse provides a holding current level.